IN THE CLAIMS:

The text of the pending claims is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please ADD new claims 21 and 22 as follows:

1. (ORIGINAL) A design system of an integrated circuit, comprising:

a timing test portion testing timing of the integrated circuit, based on circuit information and delay information indicating a circuit structure of the integrated circuit;

a circuit modification portion modifying the circuit information, based on a timing error recognized in said timing test portion;

a delay presumption portion presuming the delay information from the modified circuit information without designing layout with the circuit information modified in said circuit modification portion; and

an information update portion updating the circuit information and delay information of the integrated circuit based on the circuit information modified in said circuit modification portion and the delay information presumed in said delay presumption portion, to provide to said timing test portion.

2. (ORIGINAL) The design system of the integrated circuit according to claim 1, wherein said delay presumption portion presumes the delay information by making delay circuit models corresponding to the circuit information modified in said circuit modification portion.

3. (ORIGINAL) The design system of the integrated circuit according to claim 2, wherein the delay circuit models represent a signal propagation path between circuit elements composing the integrated circuit with a circuit of one resistance and two capacitance.

4. (ORIGINAL) The design system of the integrated circuit according to claim 1, wherein said timing test portion comprises a timing analysis portion analyzing the timing of the integrated circuit based on the circuit information and delay information of the integrated circuit, and a determination portion determining whether the timing error exists in the integrated circuit or not based on an analysis result from the timing analysis portion.

5. (ORIGINAL) The design system of the integrated circuit according to claim 1, wherein said circuit modification portion modifies the circuit information to insert circuit elements that delay a signal to a signal propagation path relating to a hold error, when the hold error is recognized in said timing test portion.

6. (ORIGINAL) The design system of the integrated circuit according to claim 5, wherein said circuit modification portion modifies the circuit information to delete the circuit elements that delay the signal, when said timing test portion recognizes set-up error appeared by modifying the circuit information to insert the circuit elements that delay the signal.

7. (ORIGINAL) A design system of an integrated circuit, comprising:

a delay presumption portion presuming delay information from modified circuit information without designing layout with the modified circuit information, when the circuit information of the integrated circuit obtaining therein the circuit information and delay information indicating a circuit structure is modified;

an information update portion updating the circuit information and delay information of the integrated circuit, based on the modified circuit information and the delay information presumed in said delay presumption portion; and

a timing analysis portion analyzing timing of the integrated circuit, based on the circuit information and delay information updated in said information update portion.

8. (ORIGINAL) The design system of the integrated circuit according to claim 7, wherein said delay presumption portion presumes the delay information by making delay circuit models corresponding to the modified circuit information.

9. (ORIGINAL) The design system of the integrated circuit according to claim 8, wherein the delay circuit models represent a signal propagation path between circuit elements composing the integrated circuit with a circuit of one resistance and two capacitance.

10. (ORIGINAL) A design method of an integrated circuit, comprising:

timing test step for testing timing of the integrated circuit based on circuit information and delay information indicating a circuit structure of the integrated circuit;

circuit modification step for modifying the circuit information to recover a timing error

when the timing error is recognized in said timing test;

delay presumption step for presuming the delay information from said modified circuit information without designing layout with the modified circuit information; and

information update step for updating the circuit information and delay information of said integrated circuit based on said modified circuit information and said presumed delay information, to test the timing of said integrated circuit.

11. (ORIGINAL) The design method of the integrated circuit according to claim 10, wherein the delay presumption step presumes, the delay information by making delay circuit models corresponding to the modified circuit information.

12. (ORIGINAL) The design method of the integrated circuit according to claim 10, wherein the circuit modification step modifies, the circuit information by inserting circuit elements that delay a signal to a signal propagation path relating to a hold error, when the hold error is recognized in said timing test.

13. (ORIGINAL) The design method of the integrated circuit according to claim 12, wherein in said timing test based on the updated circuit information and delay information of the integrated circuit, the circuit information is modified by deleting the circuit elements that delay the signal when said timing test recognizes set-up error appeared by modifying the circuit information to insert the circuit elements that delay the signal.

14. (ORIGINAL) A design method of an integrated circuit, comprising:

delay presumption step for presuming delay information from modified circuit information without designing layout with the modified circuit information, when circuit information of said integrated circuit obtaining therein the circuit information and delay information indicating a circuit structure is modified;

information update step for updating the circuit information and delay information of said integrated circuit based on the modified circuit information and said presumed delay information; and;

timing analysis step for analyzing timing of the integrated circuit based on said updated circuit information and delay information.

15. (ORIGINAL) The design method of the integrated circuit according to claim 14,

wherein the delay presumption step includes to presume the delay information by making delay circuit models corresponding to the modified circuit information.

16. (ORIGINAL) A program product for having a computer to execute the steps, comprising:

a timing test step testing timing of the integrated circuit, based on circuit information and delay information indicating a circuit structure of said integrated circuit;

a circuit modification step modifying the circuit information based on a timing error recognized in said timing test step;

a delay presumption step presuming the delay information from the modified circuit information without designing layout with the circuit information modified in said circuit modification step; and

an information update step updating the circuit information and delay information of said integrated circuit, based on the circuit information modified in said circuit modification step and the delay information presumed in said delay presumption step.

17. (ORIGINAL) The program product according to claim 16, wherein said delay presumption step presumes the delay information by making delay circuit models corresponding to the circuit information modified in said circuit modification step.

18. (ORIGINAL) The program product according to claim 16, wherein said timing test step comprises a timing analysis step analyzing timing of said integrated circuit based on the circuit information and delay information of the integrated circuit, and a determination step determining whether a timing error exists in the integrated circuit or not based on an analysis result at the timing analysis step.

19. (ORIGINAL) A program product for having a computer to execute the steps, comprising:

a delay presumption step presuming delay information from modified circuit information without designing layout with the modified circuit information, when the circuit information of the integrated circuit obtaining therein the circuit information and delay information indicating a circuit structure is modified;

an information update step updating the circuit information and delay information of the integrated circuit, based on the modified circuit information and the delay information presumed

in said delay presumption step; and

a timing analysis step analyzing timing of the integrated circuit, based on the circuit information and delay information updated in said information update step.

20. (ORIGINAL) The program product according to claim 19, wherein said delay presumption step presumes the delay information by making delay circuit models corresponding to the modified circuit information.

21. (NEW) A method for designing an integrated circuit, comprising:

testing timing of the integrated circuit based on circuit information and delay information indicating a circuit structure of the integrated circuit to recover a timing error;

modifying the circuit information to recover the timing error when the timing error is recognized in the testing;

presuming the delay information from the modified circuit information without designing a layout with the modified circuit information; and

updating the circuit information and delay information of the integrated circuit based on the modified circuit information and the presumed delay information, to test the timing of the integrated circuit.

22. (NEW) A method for designing an integrated circuit, comprising:

detecting a timing error of an integrated circuit based on first circuit information; and

presuming delay information from modified second circuit information of the integrated circuit without designing a layout with the modified second circuit information when the timing error is detected in the integrated circuit.